SQUID Module: Users Manual: **DRAFT Version**

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Supplied Voltages

Power Control Circuitry
This module utilizes the following voltages available at the backplane:

+15, -15, FE+15, FE-15 and +5D.

When the SQUID Module is plugged in, the circuitry voltages remain off for a period of approximately 1.5 seconds, after which all of the 15 volt supplies are connected to the circuitry. Approximately 300 milliseconds after application of the 15 volts, the 5D voltage is applied.

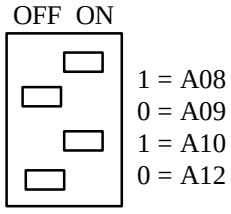
Board generated voltages.
The 4 voltages listed below are generated on board. The "Q" voltages are generated from the "FE" voltages using three terminal regulators, and are used for operating the several "Current feedback amplifiers" utilized in the signal path from input to output. The "QD" voltages are generated from the +15 and -15 voltages, and are used primarily for digital circuitry requiring "Quiet" supply voltages.

+5Q, -5Q, +5QD and -5QD.

Additionally, 4 very precise, stable voltages are generated for powering the 4 channel DAC. These voltages are +10 and -10 for power, and the +5 and -5 volts for the high and low references.

Digital Interface
In order to appear as a single gate load to the crate backplane, all of the lines are buffered. The data lines are buffered by IC34, whereas the address, read, and write lines are buffered by IC29. IC29 is operated in a unidirectional mode; always passing the backplane address, read and write signals to this module. The data lines (IC34), on the other hand, have the direction controlled by the write line, but only if this particular module is being addressed.

Module Address
The address this module responds to is determined by the address set up by switch SW4, along with IC35. SW4 as illustrated below, is set to cause this module to respond to address 0101 on address lines A12, A10,A9 & A8, respectively. (Slot 5)



SW4

Digital to Analog Converter (DAC)
This quad DAC allows the user to set the output voltage anywhere in the range of plus or minus five volts. The output voltage is given by the expression

$$Vout = -5V + (10/4096)N$$

where N is the digital word written to the DAC.

For example, if N = 0, Vo = -5 Volts. If N = 2048, Vo = 0 Volts, and if N = 4095, Vo = +4.9976 Volts.

A system reset sets the 4 outputs to zero volts. The 4 outputs control the following devices:

Module Addressing

Module Address + 0; DAC0;	Reads or writes the SQUID BIAS voltage. The output impedance is 25 kilohms. (Squid_Bias/V)
Module Address + 1; DAC1;	Reads or writes the second stage GAIN (VCON). The range varies from approximately 0.5 to 5**.** N for a gain of 5 is 0, and N for a gain of 0.5 is 1843.
Module Address + 2; **DAC2;**	Reads or writes an offset voltage (FB_Offset) into the last stage of amplification, before leaving the SQUID Module for the Driver Module, and subsequently the Data Acquisition System.
Module Address + 3; **DAC3 ;**	Reads or writes an offset voltage (Offset_ADJ) at the input of the first stage of amplification, for an adjustment of +/- 500 millivolts, for -/+ 5 volts out of the DAC.
Module Address + 4; **CSR0;**	Reads or writes the Control and status register Zero (CSR0)
Module Address + 5	A write to this address arms the zapper circuitry in the Synchronous mode, or Zaps the SQUID in the Asynchronous mode. A read to this address causes an inverted SQUID Module output signal.
Module Address + 6	A write to this address disarms the zapper circuitry in the Synchronous mode. In the Asynchronous mode, a write to this address has no effect on the zapper other than clearing the "Zapper Armed" bit in CSR0. A read to this address, produces an non-inverted, SQUID Module output signal.
. **Module Address + 7**	A write to this address causes a module reset.

Control and Status Register (CSR0), Bit assignments
The address of CSR0 is 4. The Control and Status Register consists of IC41. It is a 16 bit register with the 8 LSB's (Bit 0 through Bit 7) that can be both read from and written to, which have the following control functions:

Bit 0	calibrate/measure ["0" = Measure; "1" = Calibrate]
Bit 1	zap_mode ["0" = Asynchronous; "1" = Synchronous]
Bit 2	Zap Voltage = 2 volts["0" =0 volts; "1" = 1.25 volts]
Bit 3	Zap Voltage = 4 volts["0" = 0 volts; "1" = 2.50 volts]
Bit 4	Zap pulse width = 100 millisec.
Bit 5	Zap pulse width = 200 millisec.
Bit 6	Zap pulse width = 400 millisec.
Bit 7	Zap pulse width = 800 millisec.
Bit 8	Zapper Armed **(Read Only)** ["0" =Armed; "1" = Disarmed]
Bit 9	CSR0-09 (Not used)
Bit 10	CSR0-10 (Not used)
Bit 11	CSR0-11 (Not used)
Bit 12	CSR0-12 (Not used)
Bit 13	CSR0-13 (Not used)
Bit 14	CSR0-14 (Not used)
Bit 15	CSR0-15 (Not used)

Bit 0 calibrate/measure, puts the SQUID Module either in the "Calibrate" mode , or the "Measure" mode. In the Calibrate mode(Bit 0 = 1), IC's 5 and 9 are enabled, and the integrator (IC7, Q2 and Q3) is disabled by opening its input and placing it in the reset mode(Q3 "on"). In the Measure mode(Bit 0 = 0), the integrator, (IC7, Q2 and Q3) is placed in the integrate mode(Q3 "off"), and IC's 5 and 9 are disabled.

Bit 1 zap_mode, puts the SQUID Module either in the "Synchronous " or " Asynchronous" zapping mode.

In the asynchronous mode(CSR0, Bit 1 is low), writing to address 5 will zap the circuit.
In the synchronous mode(CSR0, Bit 1 is high), writing to address 5 will arm the zapping circuitry, causing the circuit to get zapped by a subsequent "TRIG" signal, received from the backplane. After a Synchronous zap, the zapping circuit is automatically disarmed.

Bits 2 & 3 zap_voltage, These two bits set the zap voltage for 0, 1.25, 2.5, or 3.75 Volts. Bit 2 is the LSB.

Bits 4, 5, 6, & 7 zap_width, These four bits allow the zap duration to be set for 16 different widths in 100 millisecond increments; bit 4 is the LSB.

Bit 8 Zapper arming status, This bit is read back only, and provides the status of the arming circuitry.

Bits 9 through 15 inclusive, they are unused.

Zapping Circuitry Description

The Zapping circuitry on this board provides a pulse of voltage to the SQUID which has control of both the Zap pulse, amplitude, and duration. The choice of amplitudes are 0, 1.25, 2.50, and 3.75 Volts. The choices of pulse widths are 100 to 1600 milliseconds, in 100 millisecond increments. The Zapping circuitry can be made to operate in two modes: Synchronous or Asynchronous. These modes are selected via the Control and Status Register, CSR0.

In the Synchronous mode, the Zapper is pulsed by a signal on the Trig+/Trig- lines, provided the Zapping circuitry is armed (see the section **Module Addressing)**. The absence of a trigger is determined by having the Trig+ line being at least 300 millivolts more negative than Trig-. A trigger is determined by having the Trig+ line going 300 millivolts more positive than Trig-, and will cause the Zapping circuitry to pulse. The Zapping circuitry automatically disarms itself, and must be rearmed in order to rezap the SQUID.

Leaving the Trig+ and Trig- lines float (disconnected), is interpreted by the differential receiver, as an absence of a trigger, i.e., the equivalent of the Trig+ line being at least 300 millivolts more negative than Trig- line.

In asynchronous mode, the Zapper is pulsed each time the zapper is armed (see the section **Module Addressing)**.